In the Claims:

1–21. (Cancelled)

22. (Previously Presented) A semiconductor structure from which a strained channel transistor may be fabricated, comprising:

a semiconductor substrate;

a first crystalline layer on the substrate;

a second crystalline layer on the first layer;

a trench formed in the second layer; and

a top epitaxial layer on the second layer.

23. (Original) A semiconductor structure as in Claim 22, wherein upper and lower corners of the trench are rounded.

24. (Original) A semiconductor structure as in Claim 22 wherein upper corners of the trench are rounded.

25. (Original) A semiconductor structure as in Claim 23, wherein the radii of the corners are from about 5 to about 50 nm.

26. (Original) A semiconductor structure as in Claim 22, wherein the trench has a depth of about 6,000 Å or less.

27. (Original) A semiconductor structure as in Claim 23, wherein the rounded corners are formed by heating the second layer in a gaseous ambient.

28. (Original) A semiconductor structure as in Claim 27, wherein heating is effected at a temperature within the range of about 700 C to about 950 C.

29. (Original) A semiconductor structure as in Claim 27, wherein the gaseous ambient includes O, H, N, He, Ne, Ar, Xe or a combination thereof.

30. (Original) A semiconductor structure as in Claim 27, wherein heating is effected at a pressure within the range of about 10 to about 1,000 Torr.

31. (Original) A semiconductor structure as in Claim 22, wherein the trench contains an insulative material comprising silicon oxide.

32. (Original) A semiconductor structure as in Claim 22, wherein the top layer is less than about 250 Å thick.

33. (Original) A semiconductor structure as in Claim 22, wherein the first, second and top layers comprise Si, Ge, C, or a compound semiconductor.

34. (Original) A semiconductor structure as in Claim 22, wherein the first, second and top layers comprise Si and Ge.

35. (Original) A semiconductor structure as in Claim 22, wherein

a lattice of a material of the first layer is mismatched with a lattice of the substrate; and

a lattice of a material of the second layer is mismatched with the lattice of the first layer.

36. (Original) A semiconductor structure as in Claim 35, wherein a lattice of a material of the top layer is mismatched with the lattice of the second layer.

37. (Original) A semiconductor structure as in Claim 22, wherein a free surface of one or more of the layers is planarized before a next superjacent layer is present thereon.

38. (Original) A semiconductor structure as in Claim 37, wherein planarization is effected by CMP.

39–59. (Cancelled)

60. (New) A semiconductor structure from which a strained channel transistor may be fabricated, comprising:

a semiconductor substrate;

a first crystalline layer on the substrate;

a second crystalline layer on the first crystalline layer;

a trench formed in the second crystalline layer; and

a third crystalline layer on the second crystalline layer.

61. (New) A semiconductor structure as in Claim 60, wherein upper and lower corners of the trench are rounded.

62. (New) A semiconductor structure as in Claim 60, wherein upper corners of the trench are rounded.

63. (New) A semiconductor structure as in Claim 62, wherein the radii of the corners are from about 5 to about 50 nm.

64. (New) A semiconductor structure as in Claim 60, wherein the trench has a depth of about 6,000 Å or less.

65. (New) A semiconductor structure as in Claim 62, wherein the rounded corners are formed by heating the second crystalline layer in a gaseous ambient.

66. (New) A semiconductor structure as in Claim 65, wherein heating is effected at a temperature within the range of about 700 °C to about 950 °C.

67. (New) A semiconductor structure as in Claim 65, wherein the gaseous ambient includes O, H, N, He, Ne, Ar, Xe or a combination thereof.

68. (New) A semiconductor structure as in Claim 65, wherein heating is effected at a pressure within the range of about 10 to about 1,000 Torr.

69. (New) A semiconductor structure as in Claim 60, wherein the trench contains an insulative material comprising silicon oxide.

70. (New) A semiconductor structure as in Claim 60, wherein the third crystalline layer is less than about 250 Å thick.

71. (New) A semiconductor structure as in Claim 60, wherein the first, second and third crystalline layers comprise a material selected from the group consisting essentially of Si, Ge, C, a compound semiconductor, and combinations thereof.

72. (New) A semiconductor structure as in Claim 60, wherein the first, second and third crystalline layers comprise Si and Ge.

73. (New) A semiconductor structure as in Claim 60, wherein:

a lattice of a material of the first crystalline layer is mismatched with a lattice of the substrate; and

a lattice of a material of the second crystalline layer is mismatched with the lattice of the first layer.

74. (New) A semiconductor structure as in Claim 73, wherein a lattice of a material of the third crystalline layer is mismatched with the lattice of the second crystalline layer.

75. (New) A semiconductor structure as in Claim 60, wherein a free surface of one or more of the crystalline layers is planarized before a next superjacent layer is present thereon.

76. (New) A semiconductor structure as in Claim 75, wherein planarization is effected by CMP.

77. (New) A semiconductor structure for forming a strained channel transistor, comprising:

a first layer, the first layer comprising a semiconductor substrate;

a plurality of at least four epitaxial layers on the first layer, wherein each one of the plurality has a lattice constant different from a layer below, and wherein the lattice constant difference increases with each overlaying layer of the plurality; and

a trench formed in a second epitaxial layer of the plurality.

78. (New) A semiconductor structure as in Claim 77, wherein upper and lower corners of the trench are rounded.

79. (New) A semiconductor structure as in Claim 77, wherein upper corners of the trench are rounded.

80. (New) A semiconductor structure as in Claim 79, wherein the radii of the corners are from about 5 to about 50 nm.

81. (New) A semiconductor structure as in Claim 77, wherein the trench has a depth of about 6,000 Å or less.

82. (New) A semiconductor structure as in Claim 79, wherein the rounded corners are formed by heating the semiconductor structure in a gaseous ambient.

83. (New) A semiconductor structure as in Claim 82, wherein heating is effected at a temperature within the range of about 700 °C to about 950 °C.

84. (New) A semiconductor structure as in Claim 82, wherein the gaseous ambient includes O, H, N, He, Ne, Ar, Xe or a combination thereof.

85. (New) A semiconductor structure as in Claim 82, wherein heating is effected at a pressure within the range of about 10 to about 1,000 Torr.

86. (New) A semiconductor structure as in Claim 77, wherein the trench contains an insulative material comprising silicon oxide.

87. (New) A semiconductor structure as in Claim 77, wherein a third epitaxial layer is less than about 250 Å thick.

88. (New) A semiconductor structure as in Claim 77, wherein the plurality of epitaxial layers comprise a material selected from the group consisting essentially of Si, Ge, C, a compound semiconductor, and combinations thereof.

89. (New) A semiconductor structure as in Claim 77, wherein the plurality of epitaxial layers comprise Si and Ge.